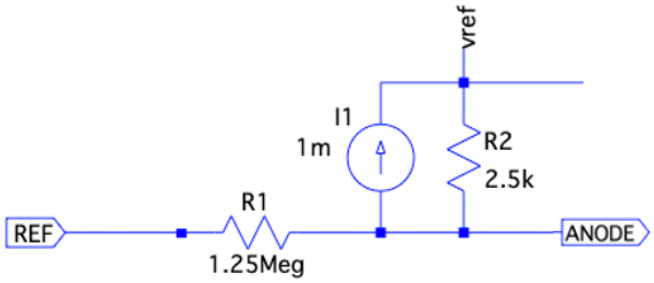
ELEC50001 EE2 Circuits and Systems

Problem Sheet 2 Solutions

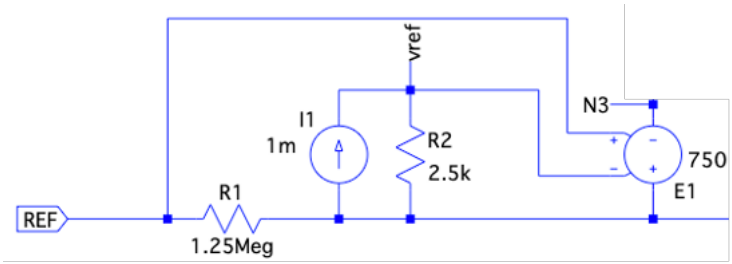
(Operation Amplifier – Modelling and Applications – Lectures 4 – 6)

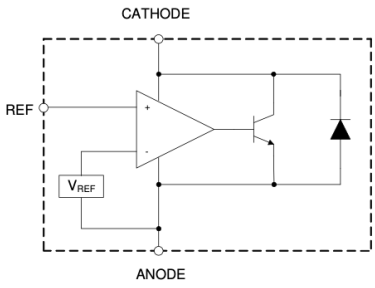
1. This question help you understand how SPICE netlist is used to model a chip. The AP431i is the voltage reference source you use in the Lab. Internally, it has a band-gap reference, an operational amplifier and an output NPN transistor to provide output current drive as an emitter follower. YOU DO NOT NEED TO KNOW how the AP431i circuit works. The purpose here is to produce a model using components specified in SPICE format to produce the behaviour of the chip reflecting the datasheet.

   (i)



   (ii) E1 ANODE N3 REF vref 750

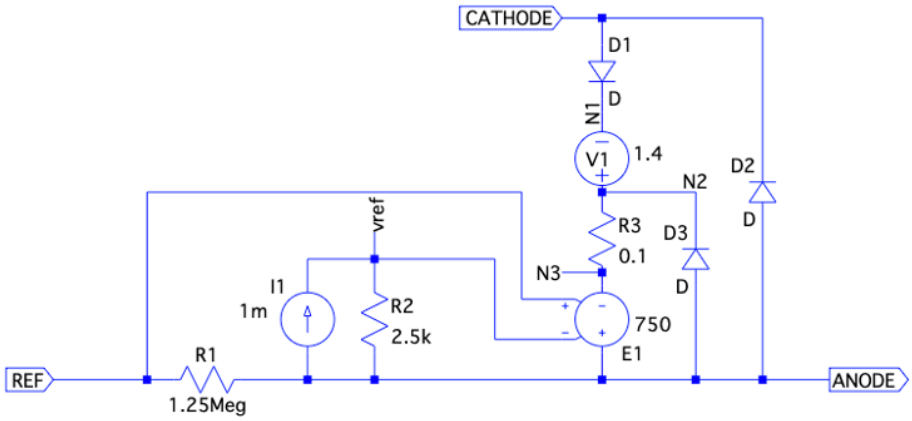




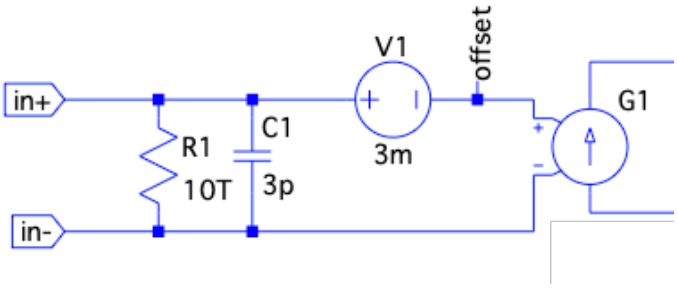
   E1 is a voltage dependent current source. The outputs of the voltage source are ANODE and N3 (internal node). The controlling voltage is between REF (+ve) and vref. The voltage gain of this is 750.

   E1 models the internal op-amp of the AP431i. The low frequency gain is 750. AP431i datasheet does not provide sufficient details. However, I know that AP431i is based on TI's TL431 design. That datasheet tells us that the DC gain is about 57dB or 750. The GBP is around 1.06MHz. However, we never use this voltage reference source as a signal amplifier. Therefore only the DC gain matters, not the GBP of the op-amp.

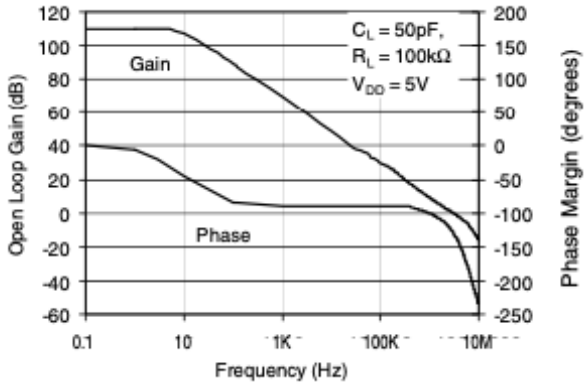
   (iii) The full model circuit is:



2. It turns out that the input stage of MCP601 has the same input impedance, but the input offset voltage over the entire temperature is ±3mV. Hence:



3. From the datasheet, we have the gain vs frequency plot. The low frequency open loop gain A_{OL} is 100dB to 115dB. This plot suggests that it is typically 110dB. The GBP is 2.8MHz.



(i), (ii) From lecture 4 slide 7, we use open-loop gain and GBP to determine R2 and gm values as follows:

$f_p = \frac{GBP}{A_{OL}} = 2.8\ x\ \frac{10^6}{316227} = 8.85Hz.$ Similar to that shown in plot.

We assume C2 = 1nF. Therefore, $R_2 = \frac{1}{2\pi f_p C_2} = 18M.$

$$gm = \frac{A_{OL}}{R_2} = \frac{316227}{17.86x10^6} = 0.018.$$

(iii). Slew rate is 2.3V/us. Given SR = max current/C2, max current = 2.3mA.

Maximum current is specified by the limit function:

```
G1 0 int_gain value={limit(0.018*V(offset, in-), 2.3m, -2.3m)}
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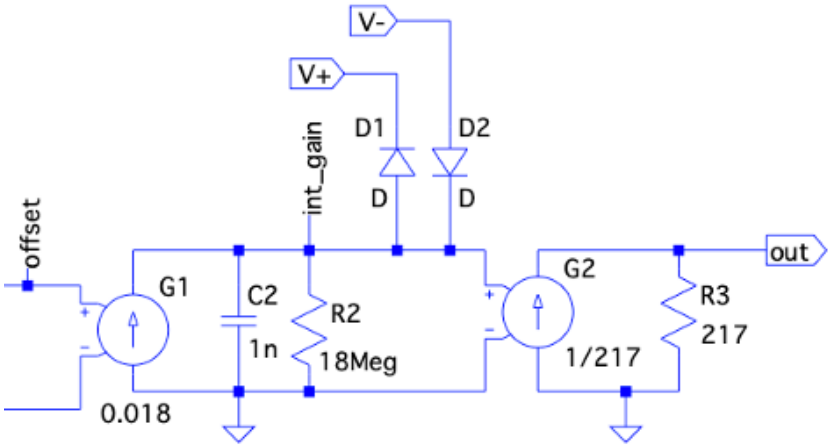
(iv). Output impedance can only be estimated from the short-circuit current. From figure 2-24 of datasheet, the short circuit current for 5.5V supply at room temperature room around 25mA. Linearly interpolate that for 5V operation gives around 23mA. 5V/23mA gives an output impedance of 217 ohms. Here is the complete circuit model (except the input stage.)



(v). Again the maximum output current cannot be shown on the schematic. The SPICE statement will be:

G2 0 out value={limit(V(int_gain, 0)/217, 23m -23m)}

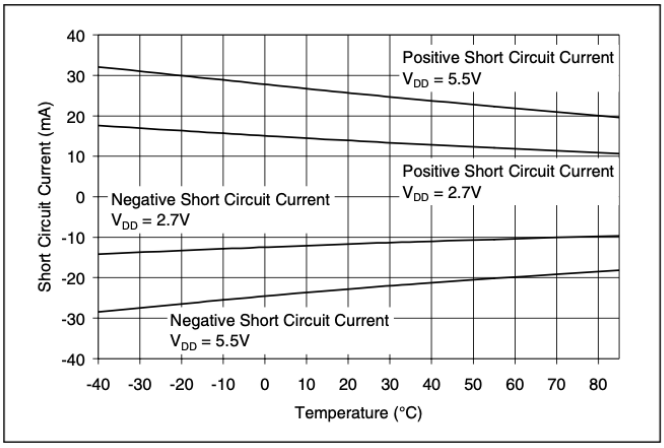


FIGURE 2-24: *Output Short Circuit Current vs. Temperature*

4. Z = [R2/(R1+R2)] * Y = X' / K (due to the negative feedback)

   Therefore X' = [R2/(R1+R2)] * K * Y

   $Y = A_1 (X - X')$

   Therefore $Y = A_1 X - A_1 * K * [R2/(R1+R2)] * Y$

   $Y\{1 + A_1 K * [R2/(R1+R2)]\} = A_1 X$

   Closed-loop gain $= \frac{Y}{X} = \frac{1}{(\frac{1}{A_1} + \frac{KR2}{R1+R2})}$

   Check: Assume A1 = infinite, K = 1, Gain = 1+ R1/R2 - correct for conventional non-inverting amplifier.

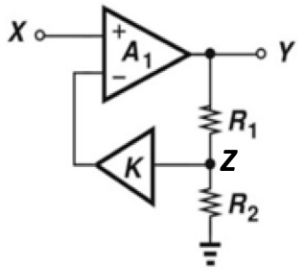


Figure Q4

5. Circuit for Q5a: Comparator output switch over state when V+ reaches V_{REF}. Apply KCL at V+ node: $(V_{IN} - V_{REF})/R1 = (V_{REF} - V_{OUT})/R2 \Rightarrow V_{IN} = (1+R1/R2)\, V_{REF} - (R1/R2) * V_{OUT}$

   For positive going V_{IN}, $V_{OUT} = 0$. Therefore $V_{th\_H} = V_{REF}\,(1+ R1/R2)$.
   For negative going V_{IN}, $V_{OUT} = 5$. Therefore $V_{th\_L} = V_{REF}\,(1+R1/R2) - 5*R1/R2$

   Circuit for Q5b: Apply KCL at node V+: $V_{IN} = V_{REF}[R2/(R1+R2)] + V_{OUT}[R1/(R1+R2)]$.

   For positive going V_{IN}, $V_{OUT} = 5$. Therefore $V_{th\_H} = V_{REF}[R2/(R1+R2)] + 5*[R1/(R1+R2))$.
   For negative going V_{IN}, $V_{OUT} = 0$. Therefore $V_{th\_L} = V_{REF}\, R2/(R1+R2)]$

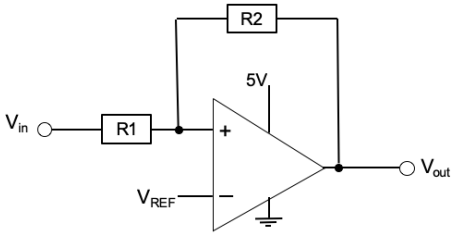


Figure Q5a

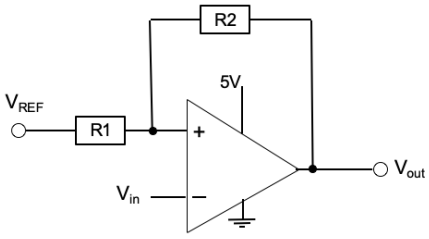


Figure Q5b

6. Apply KCL at virtual earth node:

$$\frac{V_{in}}{R_1} = -V_{out}/(R_2||Z_C)$$

$$R_2 \,||\, Z_C = \frac{R_2\left(\frac{1}{sC}\right)}{R_2 + \frac{1}{sC}} = \frac{R_2}{1 + sCR_2}.$$

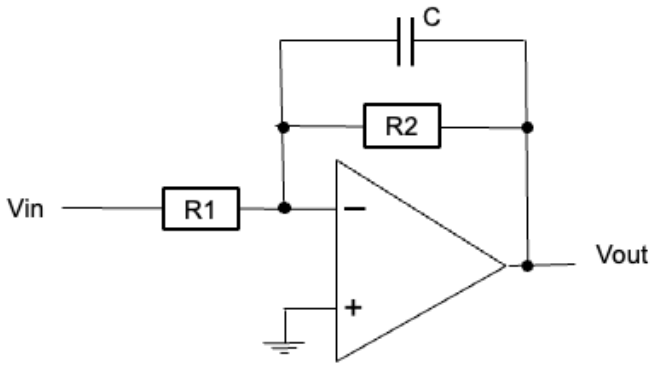
Therefore, the transfer function is:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1 + sCR_2}\right) = G(\frac{1}{1 + sCR_2})$$

where

G is gain of circuit WITHOUT capacitor = $-\left(\frac{R_2}{R_1}\right)$.

This is a low-pass filter equation with break frequency $f_b = \frac{1}{2\pi R_2 C}$.



7. Since R1 = 180k and R2 = 200k, from Q5, V_{th_H} = 4.75V and V_{th_L} = 0.25V. Therefore the triangular signal peak-to-peak is 4.5V.

For the integrator, the integration current Ic = ±(Vsq – 2.5)/R , (R = 10k).
Therefore $\Delta Vc/\Delta t$ = ic/C = 2.5/RC. ΔVc = 4.5V. Therefore Δt = RC 4.5/2.5 = 18uS. Therefore the oscillation frequency is 1 / (2* 18) MHz = 27.8kHz..

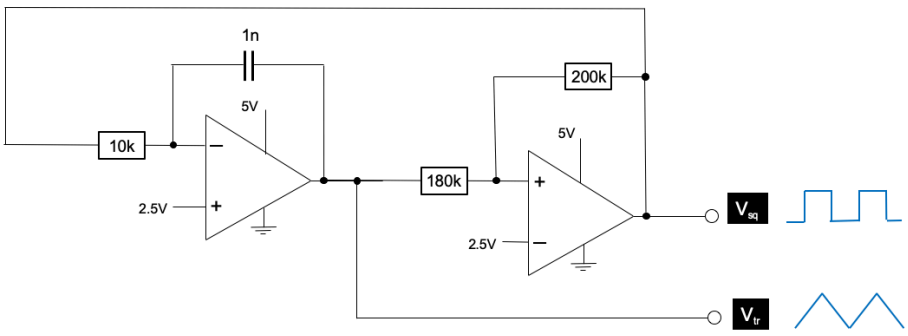


Figure Q7

8. Step 1 & 2: $f_c = 5kHz$. Therefore RC = 32us.

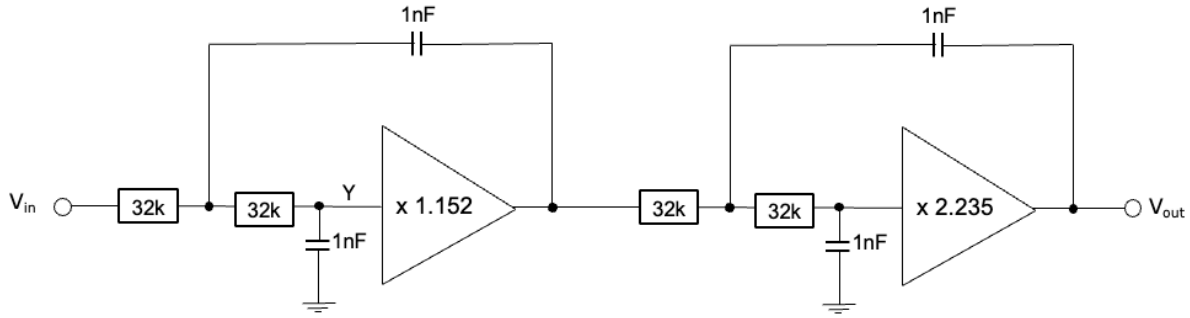
   Step 3: Pick C = 1nF.

   Step 4: Calculate R to be 32kΩ.

   Step 5 & 6: -80dB attenuation per decade implies that we require a 4th order filter. Therefore, we need two Sallen-key stages.

   Step 7: The gain of the two stages are: 1.152 and 2.235.

   Hence the filter circuit is:



9. From Lecture 6 slide 8, we have :

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{1}{\omega_0 Q}s + \frac{1}{\omega_0^2}s^2} = \frac{1}{1 + 2\boldsymbol{CR}\, s + \boldsymbol{C^2R^2}\, s^2}$$

The cut-off frequency is $fc = \frac{1}{2\pi CR}$.
Therefore,

$$R = 160k\Omega$$

$$Q = 0.5.$$

10. The triangular signal from Q5 goes from 0.25V to 4.75V. The range is 4.5V. Therefore:

Vpwm(average) =(Vin – 0.25) * (5/4.5) for 0.25 ≤ Vin ≤ 4.75.

Check: When Vin = 0.25V, Vpwm(average) = 0V (or 0% duty cycle).
When Vin = 4.75V, Vpwm(average) = 5V (or 100% duty cycle).

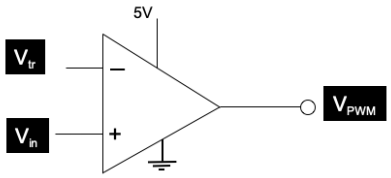


Figure Q8