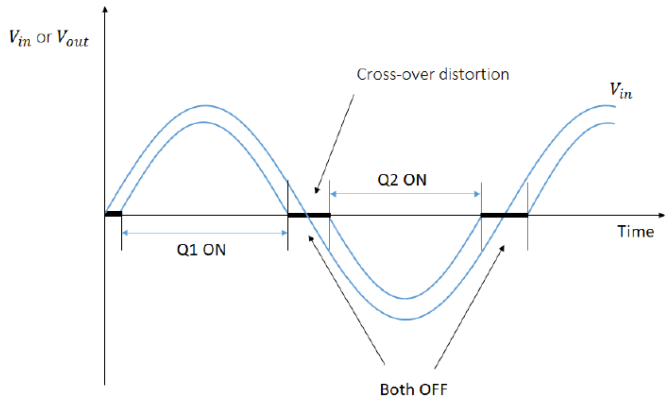
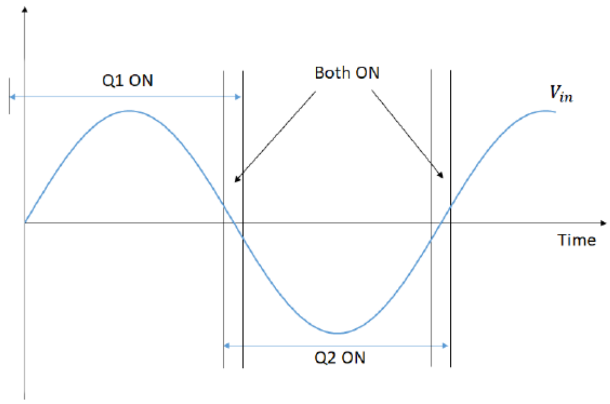
ELEC50001 EE2 Circuits and Systems

Problem Sheet 2 Solutions
(Operation Amplifier Applications – Lectures 3 – 4)

1. The circuit here is also covered in Year 1 ADC Lecture 11. Q1 and Q2 needs 0.7V in the base-emitter to make them conduct and act as emitter following for Load. So Q1a circuit waveform will look like this. (Although I discourage anyone to just remember names, this output circuit architecture is known as a Class B output.)



Adding Q1 and Q2 provides the necessary bias voltages V_{BE} for Q3 and Q4 in the circuit in Figure Q1b. R3 and R4 are small (typically 10 ohms) and they improve the linearity of the amplifier. The waveform at Vout will look something like this. There is not cross-over distortion. This is also known as a class AB output.



2. We first need to determine what determines the biasing of this transistor and hence the quiescent base current. V_{BE} is 0.7V, therefore R_B determines I_{BQ}.

$$I_{BQ} = \frac{Vcc - 0.7}{R_B} = 19.3mA$$

Therefore $I_{CQ} = \beta I_B = 25 * 19.3mA = 0.48A$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20 - 0.48 * 20 = 10.4V$$

Note that the supply current is a sinusoidal wave centred around I_{CQ}.

Therefore supply input power is:

$$P_i(dc) = V_{CC} I_{C_Q} = 20 * 0.48 = 9.6W$$

Given that input (ac) signal has a peak current of 10mA in the question, we can calculate the peak collector current:

$$I_C(pk) = \beta I_B(pk) = 250mA\ (pk)$$

Therefore ac power to load (Rc) is:

$$P_o(ac) = I_C^2(rms) R_C = \frac{I_C^2(pk)}{2} R_C = \frac{0.25^2}{2} * 20 = 0.625W$$

Hence the amplifier's power efficiency is only:

$$\eta = \frac{P_o(ac)}{P_i(dc)} = \frac{0.625}{9.6} * 100\% = 6.5\%$$

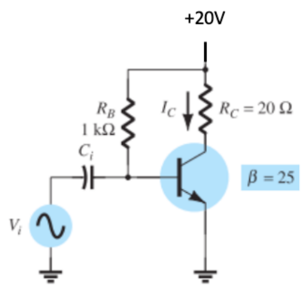


Figure Q2

3. We solve this problem in a similar way to that of Q2 except that the input power is calculated with current that is NOT the same as the quiescent current due to the push-pull action of Q1 and Q2. Instead we have to calculate the average current for the full-wave rectified current as explained in the notes.

The peak input signal voltage is:

$$V_i(pk) = \sqrt{2}\, V_i(rms) = \sqrt{2} * 12 = 17V.$$

Assuming that the voltage gain is 1. Therefore $V_L(pk) = 17V$

Hence $P_o(ac) = \frac{V_L^2(pk)}{2R_L} = \frac{17^2}{2\times 4} = 36.125W$

The peak load current is:

$$I_L(pk) = \frac{V_L(pk)}{R_L} = \frac{17}{4} = 4.25A$$

Therefore the average (dc) current draw from supply rails is:

$$I_{dc} = \frac{2}{\pi} I_L(pk) = 2 \times \frac{4.25}{\pi} = 2.71A$$

Hence power from supply is

$$P_i(dc) = V_{CC} I_{dc} = 25 \times 2.71 = 67.75W$$

The power dissipated by each of the output transistors Q1 and Q2 is the same. It is:

$$P_Q = \frac{P_i - P_o}{2} = \frac{67.75 - 36.125}{2} = 15.8W$$

The amplifier efficiency is $\eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125}{67.75} \times 100\% = 53.3\%$

This is much better than the efficiency found in Q2!

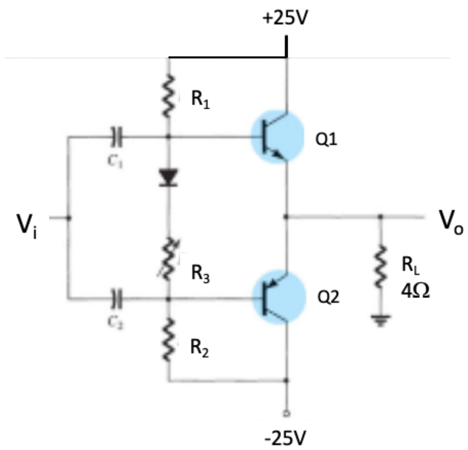


Figure Q2

4. Z = [R2/(R1+R2)] * Y = X' / K (due to the negative feedback)

Therefore X' = [R2/(R1+R2)] * K * Y

$Y = A_1 (X – X')$

Therefore $Y = A_1 X – A_1 * K *[R2/(R1+R2)] * Y$

$Y\{1 + A_1 K *[R2/(R1+R2)]\} = A_1 X$

$$\text{Closed-loop gain} = \frac{Y}{X} = \frac{1}{(\frac{1}{A_1} + \frac{KR2}{R1+R2})}$$

Check: Assume A1 = infinite, K = 1, Gain = 1+ R1/R2 - correct for conventional non-inverting amplifier.

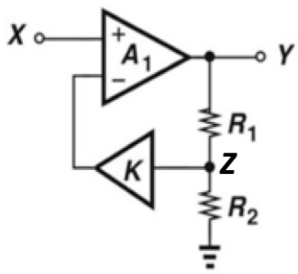


Figure Q4

5. Circuit for Q5a: Comparator output switch over state when V+ reaches V_{REF}. Apply KCL at V+ node: $(V_{IN} – V_{REF})/R1 = (V_{REF} – V_{OUT})/R2 \Rightarrow V_{IN} = (1+R1/R2) V_{REF} – (R1/R2)* V_{OUT}$

For positive going V_{IN}, $V_{OUT} = 0$. Therefore $V_{th\_H} = V_{REF} (1+ R1/R2)$.
For negative going V_{IN}, $V_{OUT} = 5$. Therefore $V_{th\_L} = V_{REF} (1+R1/R2) - 5*R1/R2$

Circuit for Q5b: Apply KCL at node V+: $V_{IN} = V_{REF}[R2/(R1+R2)] + V_{OUT}[R1/(R1+R2)]$.

For positive going V_{IN}, $V_{OUT} = 5$. Therefore $V_{th\_H} = V_{REF}[R2/(R1+R2)] + 5*[R1/(R1+R2))$.
For negative going V_{IN}, $V_{OUT} = 0$. Therefore $V_{th\_L} = V_{REF}\, R2/(R1+R2)]$

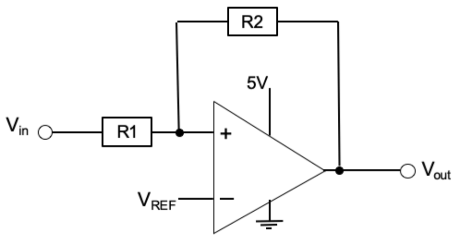


Figure Q5a

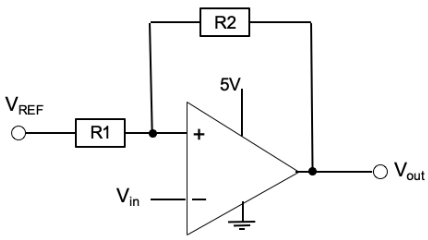


Figure Q5b

6. Since R1 = 180k and R2 = 200k, from Q5, V_{th_H} = 4.75V and V_{th_L} = 0.25V. Therefore the triangular signal peak-to-peak is 4.5V.

   For the integrator, the integration current Ic = ±(Vsq – 2.5)/R , (R = 10k).
   Therefore ΔVc/Δt = ic/C = 2.5/RC. ΔVc = 4.5V. Therefore Δt = RC 4.5/2.5 = 18uS. Therefore the oscillation frequency is 1 / (2* 18) MHz = 27.8kHz..

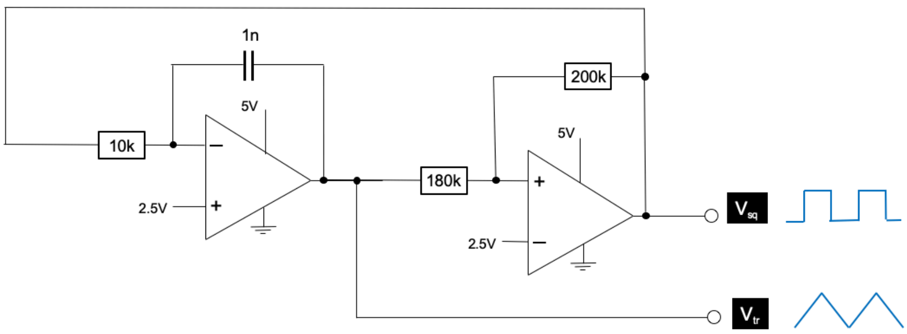


Figure Q6

7. $$\frac{Vout(s)}{Vin(s)} = \frac{1/R1R2C1C2}{s^2+s\left(\frac{1}{R2C1}+\frac{1}{R1C1}\right)+\frac{1}{R1C1R2C2}}$$

For Butterworth filter, the cut-off frequency is $fc = \frac{1}{2\pi\sqrt{R1R2C1C2}}$

Since C1 = C2 = 10nF, R1 = R2 = 1.59k ohm.

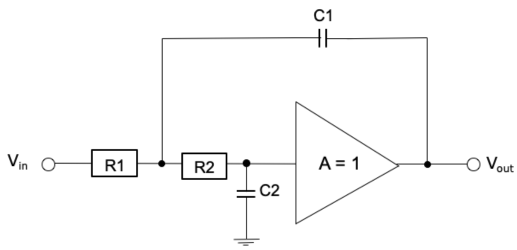


Figure Q7

8. The triangular signal from Q5 goes from 0.25V to 4.75V. The range is 4.5V. Therefore:

   Vpwm(average) =(Vin – 0.25) * (5/4.5) for 0.25 ≤ Vin ≤ 4.75.

   Check: When Vin = 0.25V, Vpwm(average) = 0V (or 0% duty cycle).
   When Vin = 4.75V, Vpwm(average) = 5V (or 100% duty cycle).

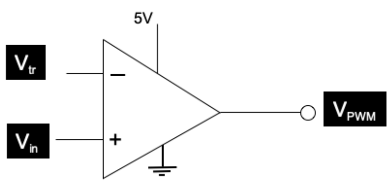


Figure Q8